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POWER STROBING

Today's memory technology is tending towards the use of larger and faster memory systems and at the same time is becomming more demanding with respect to power economy. This article will discuss the means by which significant power reduction can be obtained in a memory system while maintaining a reasonable degree of speed.

Specifically, the method here will be power strobing. In power strobing, average power consumption is reduced by applying Vcc supply to the memory device(s) only during access, and removing it during memory de-select.

Only power strobing of bipolar ROM's will be considered since they lend themselves particularly well to this type of application. The reason for this is that bipolar ROM circuits have low access times, have relatively high power consumption and are non-volatile. This will give us overall system speed as well as considerable efficiency in the use of power strobing. Also, to reach maximum power economy, supply voltage should be dropped to zero volts when powering down the memory device which can only be done if the device is non-volatile.

D.C. PARAMETERS

Removing Vcc completely from the memory circuit during de-select raises some question as to the behavior of DC input and output parameters, especially for Vcc equals 0V.

In choosing a device to be power strobed a look must be taken first at the input currents, both for an applied high and for an applied low state at the input. It is necessary that the input impedance remain high and not display any radical changes over an extended Vcc range going from 0V to 5V. It might then be convenient to define three DC input currents: $(I_{IL})_M$, $(I_{IH})_\emptyset$, and $(I_{IH})_M$. Respectively: input current with low level applied, Vcc = (Vcc)max; input current with high level applied, Vcc = 0V (disconnected); and input current with high level applied, Vcc = (Vcc)max. $(I_{IL})_M$ and $(I_{IH})_M$ are the normally defined input currents and should be found in the device data sheets.

Similarly, device output leakage currents must remain within limits both during "power-up" and during "power-down". This will ensure that the outputs are truely off during de-select even though Vcc has been removed.

For an open collector device we could define two output leakage currents: $(I_{OLH})_\emptyset$ and $(I_{OLH})_M$. Respectively: output leakage current with high level applied, Vcc = 0V; and output leakage current, high level applied, Vcc = (Vcc)max.

For tri-state, one additional current would be needed in order to specify upper string leakage. We could have then, $(I_{OLL})_M$ defined as output leakage current, low level applied, Vcc = (Vcc)max.

SUMMARY OF DEFINITIONS:

PARAMETER	DEFINITION	REMARKS
$(I_{IL})_M$	Input "low" current, Vcc = (Vcc)max.	Data Sheet Parameter
$(I_{IH})_\emptyset$	Input leakage current, Vcc = 0V	
$(I_{IH})_M$	Input leakage current, Vcc = (Vcc)max.	Data Sheet Parameter
$(I_{OLH})_\emptyset$	Output leakage, high level applied (to output), Vcc = 0V	
$(I_{OLH})_M$	Output leakage, high level applied, Vcc = (Vcc)max.	Data Sheet Parameter
$(I_{OLL})_M$	Output leakage, low level applied, Vcc = (Vcc)max.	Data Sheet Parameter

AC PARAMETER

The circuit schematic in figure 1 is a general block diagram for any power strobing circuit (using one memory device) and will be used to define AC parameters. Refer to figure 2 for waveforms.

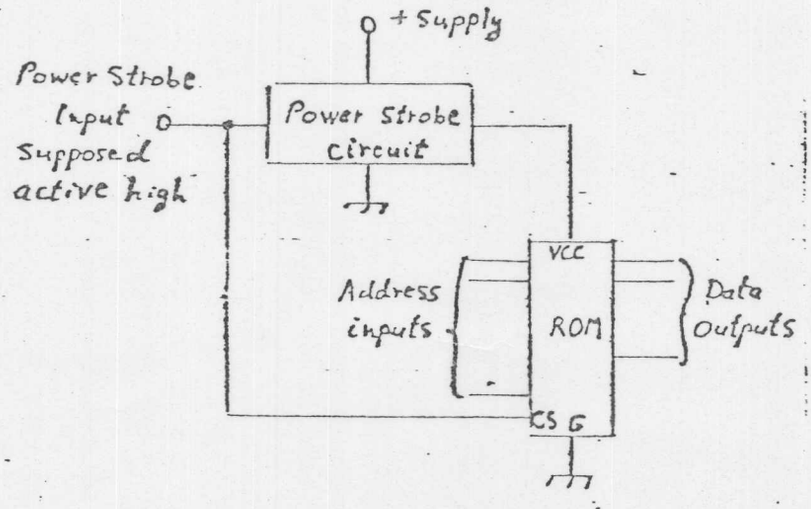

FIGURE 1

DEFINITIONS

1. TSA (Strobe Access Time) — Time delay measured from active edge of power strobe input to valid data output, measured between 50% points.

2. TSD (Strobe Disable Time) — Time delay measured from negative edge of power strobe input to output disable.

   NOTE: pull-up resistors are used for AC testing.

3. TAS (Address to Strobe Set-Up Time) — Time interval between edge of valid address and active edge of strobe input. Interval is measured between 50% points and is positive if address edge precedes strobe input edge.

4. TAH (Address to Strobe Hold Time) — Time interval between disable edge of strobe input and next cycle address edge. Measured between 50% points and positive if strobe edge precedes address edge.

For reference we can define:

5. TSON (Strobe to Power On) — Time delay measured from active edge of strobe input to positive edge of Vcc supply voltage applied to device measured from 50% to 50%.

6. TSOF (Strobe to Power Off) — Time delay measured from disable edge of strobe input to negative edge of Vcc supply voltage applied to device. Measured from 50% to 50%.

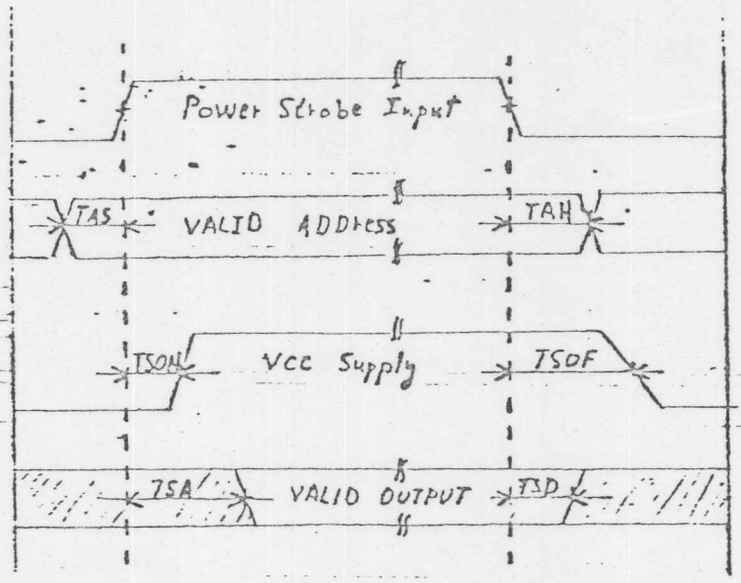

FIGURE 2

METHODS OF POWER STROBING

1. PNP Saturated Switching

A technique for power strobing a ROM (PROM) memory using a PNP saturated switch is shown in figure 3.

Saturated switching provides control of Vcc without the need for auxilary power supply voltages. The power strobe input and chip select (active high) are tied together providing faster memory "turn-off" during power-down. In the case where the ROM chip select is active low the NAND gate in the schematic is substituted for ¼ 7409 (AND function). The power strobe input then becomes active low.

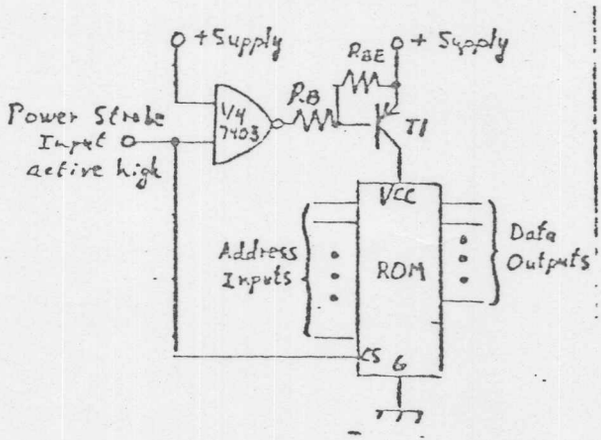

FIGURE 3

Transistor T1 should be chosen for high switching speeds, low saturation voltage, good current gain (β), and a maximum collector rating well above the ROM's Icc.

The (+) supply voltage should be 5.0V plus the saturation voltage (V_{CE})sat across T1.

Resistor RBE is non-critical and can have a value in the neighborhood of 5K .

Resistor RB can be calculated using:

$$RB = \frac{10 \times [\ (+)\ \text{Supply} - (VEB)\text{sat} - 0.4V\ ]}{Icc}$$

Where:
- (VEB)sat = emitter-base saturation voltage for T1.
- Icc = ROM supply current consumption

Example:
- (+) supply = 5.5V
- (VEB)sat = 0.7V
- Icc = 130mA

[RB = 339Ω]

2. Harris HD-6600 Quad Power Strobe

A circuit employing Harris HD-6600 quad power strobe integrated circuit to selectively apply Vcc to one-of-four ROM memory circuits is shown in figure 4. Here, the power strobe input signal is active low, and the active low chip enables from each ROM are tied to the corresponding HD-6600 input in order to speed up memory "turn-off" during power-down.

Note, that in this circuit it is necessary to use an auxiliary 12V power supply for Vcc2.

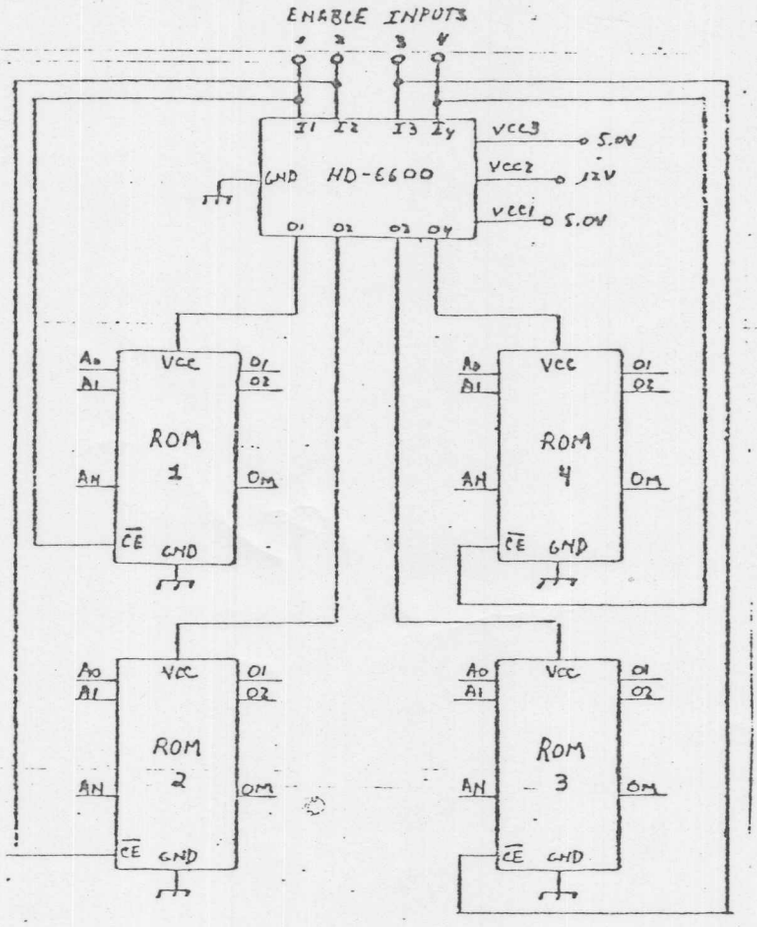
ENABLE INPUTS
1
2
3
4
I1 I2 I3 I4
VCC3
5.0V
GND HD-6600
VCC2
12V
VCC1
5.0V
O1 O2 O3 O4
A0
A1
AN
VCC
O1
O2
OM
ROM 1
ROM 2
ROM 3
ROM 4
CE
GND

FIGURE 4

APPLICATIONS TO THE SIGNETICS 82S115, 4K P/ROM

1. P/ROM Description

A complete description of the 82S115 (as well as the 82S114) can be found in the Signetics data sheet. Briefly, however, the 82S115 is a 4096-bit bipolar field programmable ROM organized as 512 words of 8 bits. The circuit is fully TTL compatible and has tri-state outputs. Two complementary chip enables (CE1 and CE2) are included for use in memory expansion and power strobing. The circuit also contains an 8 bit output register controlled by the "strobe" input pin. (No connection to power strobing).

2. DC Performance

As was discussed under "DC parameters" we must first be certain that leakage currents remain low both at the input and output of the device when Vcc is removed. Measurements made on a curve tracer show that $(I_{IH})_{\emptyset}$ (input leakage current, high level applied to input under test, Vcc removed) and $(I_{OLH})_{\emptyset}$ (output leakage current, high level applied to output under test, Vcc removed) to be less than the maximum values specified in the data sheet for the same parameter measured with Vcc applied.

3. Power Strobing the 82S115 Using a PNP Saturated Switch

The circuit of figure 3 is directly applicable to the 82S115 and is redrawn in figure 5. Three hundred ohm pull-up resistors (to +5V) are used on the outputs to force them to logic "1" during turn-off. Note, that if there were several 82S115 circuits which were wire - or'd, the outputs would always be at a defined state without the need for pull-ups so long as one of the memories were enabled.

Figure 6 shows input and output waveforms as they would appear during testing.

As can be seen in the diagram, address-strobe set-up time and address-strobe hold time were set to ONS, (TAS = TAH = ONS). Increasing address set-up time beyond ONS does not effect TSA (Strobe Access Time). Worse case TSA (Strobe Access) is 100NS for all possible address transitions. Address generation was done using a "gallop" pattern.

Vcc supply voltage rises to its 50% point in about 35NS from power strobe enable. However, it takes over a micro-second for Vcc to fall to 50% of its value once power strobe input becomes low. This is because no form of pull-down is used to remove Vcc from the device. An active pull-down could be used, but this would be at the expense of more circuitry. Also, supply current spiking could result during switching because of unequal turn-on and turn-off times between the pull-up and pull-down transistors. A resistive pull-down on the other hand would increase power consumption. The best way of handling the slow Vcc turn-off is to disable the memory through the chip select (enable) line at the same time we remove power. In this way, turn-off results in 30NS.

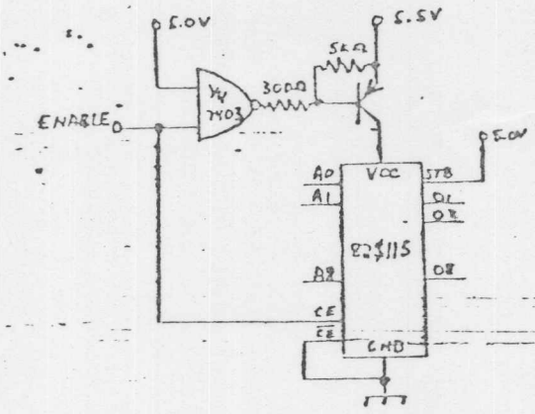

FIGURE 5

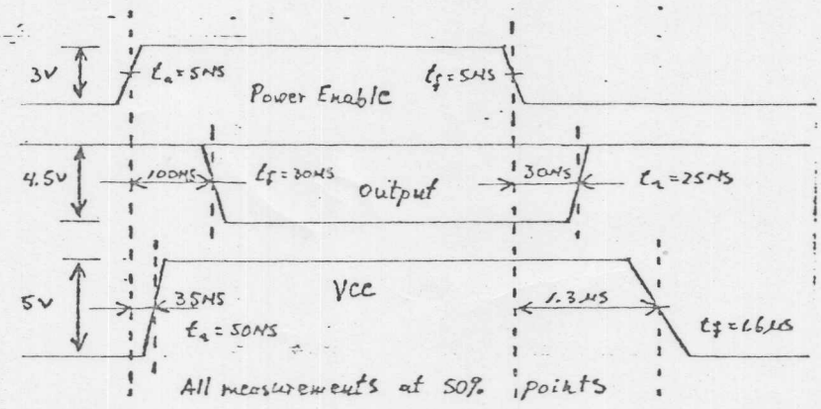

FIGURE 6

PARAMETER	DEFINITION	MAXIMUM VALUE (nominal supply, room temperature)
TSA	Strobe Access Time	100ns
TSD	Strobe Disable	30ns
TAS	Address to Strobe Set-Up	0ns
TAH	Address to Strobe Hold	0ns
TSON	Strobe to Power On	35ns
TSOF	Strobe to Power Off	1-2us

POWER STROBING THE 82S115 USING THE HARRIS HD-6600

The circuit in figure 4 is also directly applicable to the 82S115 and is redrawn in figure 10. Here, the active low chip enable is used and the ROM internal strobe input is tied high for transparent read mode. The maximum 82S115 Icc of 185mA is safely below the 200mA drive capability for each of the four HD-6600 outputs.

Experimental data was taken on the circuit of figure 11 using recommended operating conditions for the HD-6600 (Vcc1 = 5v, Vcc2 = 12v, Vcc 3 = 5v). Pull-up resistors of 300Ω each to 5.0v were connected to the eight ROM outputs. The waveforms obtained are drawn in figure 12.

SUMMARY OF RESULTS

TSA	–	105ns
TSD	–	30ns
TAS	–	0ns
TAH	–	0ns
TSON	–	40ns
TSOF	–	60ns

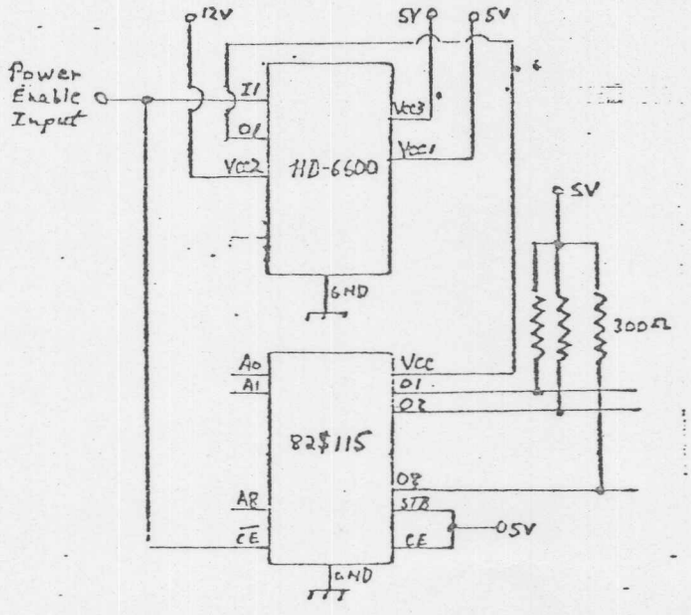

FIGURE 10

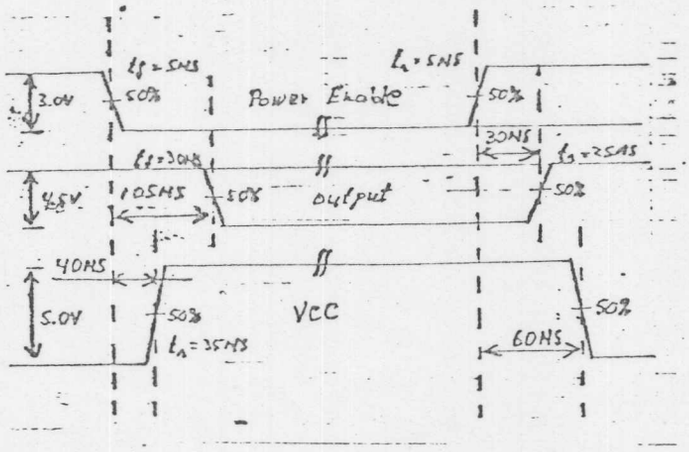

FIGURE 11

POWER SAVINGS VERSUS MEMORY ORGANIZATION AND DUTY CYCLE

WORD ORGANIZED MEMORY SYSTEM

Consider the memory system in figure 12 consisting of Nw rows and Nb columns. Each memory IC is organized as W words of B bits. The total system is then, $N_w \cdot W$ words of $N_b \cdot B$ bits.

Individual system words are obtained by power strobing a row of memory circuits on and by selecting an address. If we suppose that only one row of memory circuits remains on at a time, then the power savings with respect to the same system without power strobe is:

$$\text{Power Savings} = P_1 N_b N_w - P_1 N_b$$

where, P_1 = Power consumption of one memory IC.

and,

$$\% \text{ Power Savings} = \frac{100 \times (P_1 N_b N_w - P_1 N_b)}{P_1 N_b N_w} = 100 - \frac{100}{Nw}$$

Power savings increases as the number of rows in the memory system is made to increase.

EXAMPLE:

4K Memory X 16 bits — $N_w = 8$; $N_b = 2$

[% Savings = $100 - \frac{100}{8} = 100 - 12.5 = 87.5\%$]

$W = 512$, $B = 8$

LOW DUTY CYCLE AND POWER SAVINGS

In many applications a memory device need only be turned on for short periods of time during which data is taken out of the device and used or stored elsewhere. Figure 13 shows a generalized timing diagram for which a device is only on for Te seconds during a particular system cycle. Suppose this system cycle to be Ta seconds in length and that there be series of cycles (dead cycles) where the memory isn't needed at all. Referring to figure 13 and considering all sequences of active and dead cycles to be repetitive we have:

$$\text{Average Power} = \frac{P_1 T_e N_a}{T_a(N_a + N_d)}$$

where, P_1 = memory power consumption.

Power savings then, with respect to the same memory device without power strobing is:

$$\text{Power Savings} = P_1 \cdot \left(1 - \frac{T_e N_a}{T_a(N_a+N_d)}\right)$$

And,

$$\% \text{ Power Savings} = 100 \times \left(1 - \frac{Te \cdot Na}{Ta \cdot (Na+Nd)}\right)$$

EXAMPLE:

Te = 200ns; Ta = 1us; Nd = 2 X Na —— % Power Savings = 90%

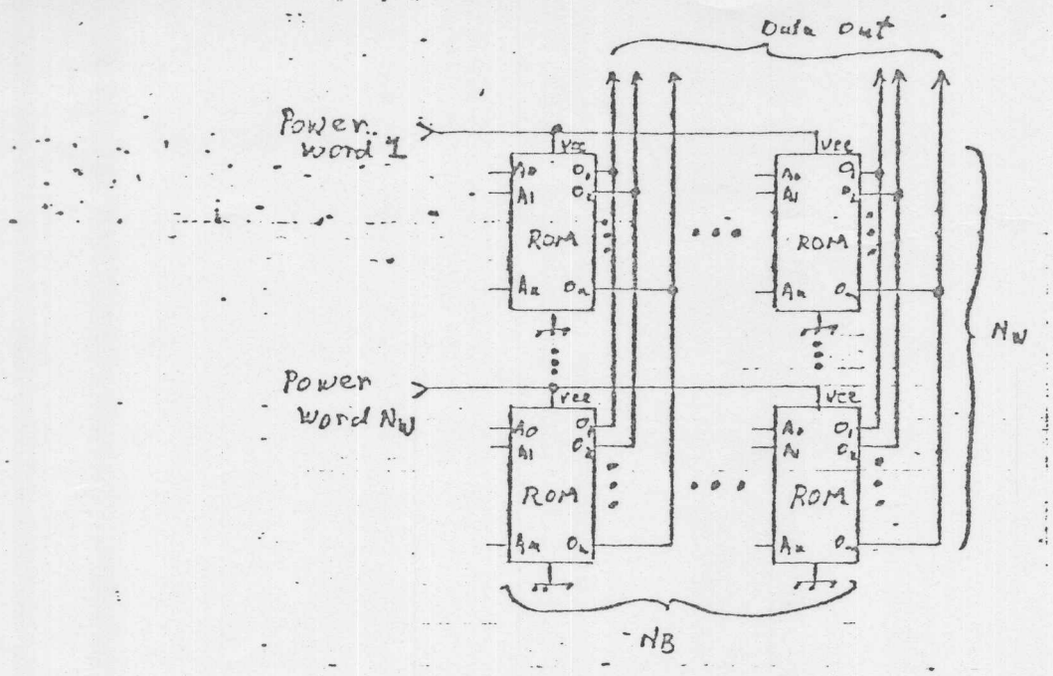

FIGURE 12

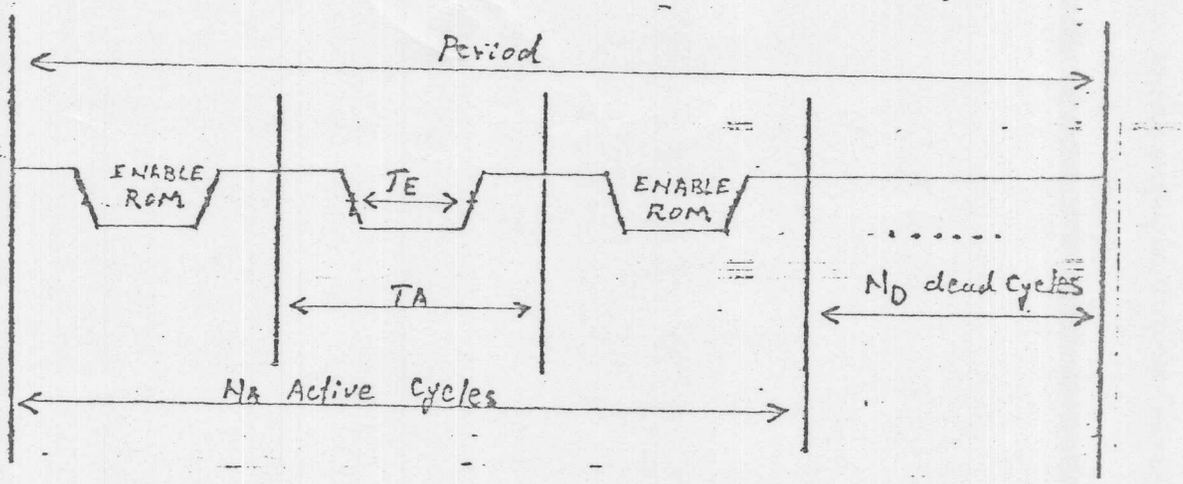

FIGURE 13